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| **Module Code** | **EEU33C07** |
| **Module Name** | Digital Systems Design |
| **ECTS Weighting**[1] | 5 ECTS |
| **Semester taught** | Semester 2 |
| **Module Coordinator/s** | Assistant Professor Shreejith Shanker, Assistant Professor George Floros |
| **Module Learning Outcomes with reference to the Graduate Attributes and how they are developed in discipline** | On successful completion of this module, students should be able to:<br><br>1. Discriminate between combinatorial and sequential circuits.<br>2. Design state machines to control complex systems.<br>3. Understand digital design flows for systems design and evaluate the trade-offs involved in different approaches.<br>4. Write synthesisable Verilog.<br>5. Write Verilog testbenches to test Verilog modules.<br>6. Write test cases and high-level test plans.<br>7. Target a Verilog design to an FPGA board.<br>8. Analyse and debug Verilog modules.<br><br>The module is highly practical. Students are expected to be self-motivated and demonstrate the learning process by preparing and engaging in lab sessions, assignments and additional course materials. This module forms the foundation for the Integrated Circuits Design course in Senior Sophister.<br><br>**Graduate Attributes: levels of attainment**<br>To act responsibly - Enhanced<br>To think independently - Attained<br>To develop continuously - Enhanced<br>To communicate effectively - Attained |

[1] TEP Glossary

**Module Content**

The student will need to re-familiarise themselves with computer arithmetic from 1st year. Topics studied in 3C7:

- In-depth study of combinatorial and sequential logic and finite state machines.
- Digital design flows and design trade-offs.
- FPGA architecture and resources.
- Verilog HDL language.
- Vitis (Vivado) design and simulation environment.
- Testbench construction.
- Realisation of all above concepts in hardware designs.

**Teaching and Learning Methods**

This is a highly practical module. There will be 2 "classic" style lectures per week. There will also be a two-hour practical session each week which will be a lecture-come-lab, where the lecturer will talk about the content of the session and the student will "learn by doing". The FPGA board used to support the practical sessions is the Basys-3 Artix-7 FPGA board. The practical sessions will require the students to complete the weekly assignment outside class hours, spreading the load through the year. It is critical that the student keeps up with the practical work during the semester.

**Assessment Details**[2]
**Please include the following:**

- **Assessment Component**
- **Assessment description**
- **Learning Outcome(s) addressed**
- **% of total**
- **Assessment due date**

| Assessment Component | Assessment Description | LO Addressed | % of total | Week due |
|---|---|---|---|---|
| Lab Quiz/Viva | Quiz/Viva in lab | 1, 3, 4, 5, 6, 8 | 10 | Week 8/9 |
| Assignments | Design exercises | 2-8 | 40 | Week 7, 11 (Semester 2) |
| Final Exam | End of year exam | All | 50 | As per timetable |

**Reassessment Requirements**

100% based on Exam

**Contact Hours and Indicative Student Workload**[2]

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| **Contact hours:**<br>44 hours (22 hr lecture, 22 hr lab) |
| **Independent Study (preparation for course and review of materials):**<br>2 hours lab prep/completion/writeup (formative) [14]<br>2 hour / week for lecture review/self study [24] |
| **Independent Study (preparation for assessment, incl. completion of assessment):** |

[2] TEP Guidelines on Workload and Assessment

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|---|---|
| | 4 hours per assignment [8]<br>Exam Preparation 10-25 hours |
| **Recommended Reading List** | 1. FPGA Prototyping By Verilog Examples: Xilinx Spartan-3 Version, Pong P. Chu (wiley).<br>2. Verilog HDL, 2/e Palnitkar (reference only). |
| **Module Pre-requisite** | EE1E6 or equivalent |
| **Module Co-requisite** | |
| **Module Website** | On Blackboard |
| **Are other Schools/Departments involved in the delivery of this module? If yes, please provide details.** | |
| **Module Approval Date** | |
| **Approved by** | Prof. Naomi Harte |
| **Academic Start Year** | September 2025 |
| **Academic Year of Date** | 2025/2026 |