Module Code	EEU33C08		
Module Name	Digital Circuits Design		
ECTS Weighting <sup>2</sup>	5 ECTS		
Semester taught	Semester 2		
Module Coordinator/s	Mr. Eugene O'Rourke		
Module Learning Outcomes with reference to the Graduate Attributes and how they are developed in discipline	On successful completion of this module, students should be able to:  Describe and plan a project involving digital electronics.  Construct a hardware solution for a digital electronics problem.  Sketch a block diagram of the circuit along with user interfaces.  Select a definite test strategy to check each stage of the design.  Obtain and describe timing waveforms.  Write a structured comprehensive technical report on the project.  Work as part of a team.  Graduate Attributes: levels of attainment  To act responsibly - Enhanced  To think independently - Enhanced  To develop continuously - Enhanced  To communicate effectively - Enhanced		
Module Content	<ul> <li>Please provide a brief overview of the module of no more than 350 words written so that someone outside of your discipline will understand it.</li> <li>Fundamental building blocks of digital circuits from gates to system level devices.</li> <li>Frequently used important blocks like decoders, multiplexors, flipflops, shift registers, counters and timers.</li> <li>Use of block diagrams, circuit schematics with MULTISIM, circuit simulation &amp; testing.</li> <li>Use of micro-controllers (Arduino) to implement tests of various stages of the electronic circuit.</li> <li>Analysis and design of combinational &amp; synchronous digital systems.</li> <li>Design partitioning</li> <li>Planning &amp; scheduling a project</li> <li>Maintaining good engineering documentation.</li> </ul>		

 $<sup>^{1}</sup>$  <u>An Introduction to Module Design</u> from AISHE provides a great deal of information on designing and re-designing modules.

<sup>&</sup>lt;sup>2</sup> TEP Glossary

#### **Teaching and Learning Methods**

Lecture & laboratory, practice-based.

The hardware construction of two real working circuits is required – one introductory project, and one more challenging circuit. The project is launched from introductory laboratory exercises with CMOS ICs. Support is on hand from the demonstrator and technical officers throughout the project.

## Assessment Details<sup>3</sup>

## Please include the following:

- Assessment Component
- Assessment description
- Learning Outcome(s) addressed
- % of total
- Assessment due date

- dd	Assessment Component	Assessment Description	LO Addressed	% of total	Week due
	Project 1 Report	Individual 5 page Report	ALL	10%	Week 26
	Project 2 Demo	Group Demonstrati on & Interview	ALL	40%	Week 33
	Project 2 Report	Individual 10 page Report	ALL	50%	Week 34

#### **Reassessment Requirements**

Exam and/or Repeat Project (8 hour day in EE-AAP Undergraduate laboratory, 9AM to 1PM & 2PM to 6PM to design, capture, simulate & verify, build & test, demonstrate & present a project arbitrarily chosen by course coordinator)

# Contact Hours and Indicative Student Workload<sup>3</sup>

### **Contact hours:**

30 Hours(Normally 33, but lose a day to 2020 Bank Holiday)

Independent Study (preparation for course and review of materials):

10 Hours

Independent Study (preparation for assessment, incl. completion of assessment):

80 Hours

## **Recommended Reading List**

**1:** Horowitz, P & Hill, Winfield, The Art of Electronics, 3<sup>rd</sup> ed. Cambridge University Press. 2015.

**2:** Katz, R. & Boriello, G., *Contemporary Logic Design*, 2<sup>nd</sup> ed. Pearson Education. 2005.

**3:** Hodges D. A. & Jackson H. G., *Analysis & Design of Digital Integrated Circuits*, 2<sup>nd</sup> ed. McGraw-Hill; 1988.

<sup>&</sup>lt;sup>3</sup> TEP Guidelines on Workload and Assessment

Module Pre-requisite	Intermediate Multisim Proficiency
Module Co-requisite	Intermediate Breadboard, Multimeter & Oscilloscope Debugging Proficiency
Module Website	https://www.tcd.ie/Engineering/undergraduate/baiyear3/modules/3C8.pdf
Are other Schools/Departments involved in the delivery of this module? If yes, please provide details.	NO
Module Approval Date	
Approved by	
Academic Start Year	
Academic Year of Date	