Module Template for New and Revised Modules[1]

Module Code	**EEU33C07**
Module Name	Digital Systems Design
ECTS Weighting[2]	5 ECTS
Semester taught	Semester 1
Module Coordinator/s	Assistant Professor Shreejith Shanker
Module Learning Outcomes with reference to the Graduate Attributes and how they are developed in discipline	On successful completion of this module, students should be able to: 1. Discriminate between combinatorial and sequential circuits. 2. Design state machines to control complex systems. 3. Define and describe digital design flows for system design and recognise the trade-offs involved in different approaches. 4. Write synthesisable Verilog. 5. Write a Verilog testbench to test Verilog modules. 6. Analyse code coverage of a Verilog testbench. 7. Target a Verilog design to an FPGA board. 8. Analyse and debug Verilog modules. The module is highly practical. Students are expected to be self-motivated and demonstrate the learning process by preparing and engaging in lab sessions, assignments and additional course materials. This module forms the foundation for the Integrated Circuits Design course in Senior Sophister. **Graduate Attributes: levels of attainment** To act responsibly - Enhanced To think independently - Attained To develop continuously - Enhanced To communicate effectively - Attained

[1] An Introduction to Module Design from AISHE provides a great deal of information on designing and re-designing modules.
[2] TEP Glossary

Module Content

The student will need to re-familiarise themselves with computer arithmetic from 2nd year. Topics studied in 3C7:

- In-depth study of combinatorial and sequential logic and finite state machines.
- Digital design flows and design trade-offs.
- FPGA structure and design flow.
- Verilog HDL language.
- Vivado simulation environment.
- Testbench construction.
- Realisation of all above concepts in hardware designs.

Teaching and Learning Methods

This is a highly practical module. There will be 2 "classic" style lectures per week. There will also be a two-hour practical session each week which will be a lecture-come-lab, where the lecturer will talk about the content of the session and the student will "learn by doing". The FPGA board used to support the practical sessions is the Basys-3 Artix-7 FPGA board. The practical sessions will require the students to complete the weekly assignment outside class hours, spreading the load through the year. It is critical that the student keeps up with the practical work during the semester.

Assessment Details[3]
Please include the following:

- **Assessment Component**
- **Assessment description**
- **Learning Outcome(s) addressed**
- **% of total**
- **Assessment due date**

Assessment Component	Assessment Description	LO Addressed	% of total	Week due
Lab	FPGA design lab	4, 5, 6, 7, 8	10	1 week after lab
Assignments	Design exercises	2-8	40	Week 7, 11 (Semester 1)
Final Exam	End of year exam	All	50	As per timetable

Reassessment Requirements

100% based on Exam

Contact Hours and Indicative Student Workload[3]

Contact hours: 44 hours (22 hr lecture, 22 hr lab)
Independent Study (preparation for course and review of materials): 2 hours lab prep/completion/writeup (formative) [14]

[3] TEP Guidelines on Workload and Assessment

	2 hour / week for lecture review/self study [24] **Independent Study (preparation for assessment, incl. completion of assessment):** 4 hours per assignment [8] Exam Preparation 10-25 hours
Recommended Reading List	1. FPGA Prototyping By Verilog Examples: Xilinx Spartan-3 Version, Pong P. Chu (wiley). 2. Verilog HDL, 2/e Palnitkar (reference only).
Module Pre-requisite	EE1E6 or equivalent
Module Co-requisite	
Module Website	On Blackboard
Are other Schools/Departments involved in the delivery of this module? If yes, please provide details.	
Module Approval Date	
Approved by	
Academic Start Year	13th September 2021
Academic Year of Date	2021/22