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| <b>Module Code</b>   | <b>EE5M02</b>   |
| <b>Module Name</b>   | Microelectronic Circuits  |
| <b>ECTS Weighting<sup>2</sup></b>  | 5 ECTS  |
| <b>Semester taught</b>   | Semester 2  |
| <b>Module Coordinator/s</b>  | Dr Justin King  |
| <b><u>Module Learning Outcomes</u> with reference to the <u>Graduate Attributes</u> and how they are developed in discipline</b> | <p>On successful completion of this module, students should be able to:</p> <p>LO 1: Explain the electrical operation of the metal-oxide-semiconductor (MOS) field effect transistor.</p> <p>LO 2: Analyse the fundamental static and dynamic performance of simple CMOS circuits noting design trade-offs.</p> <p>LO 3: Implement various CMOS logic structures.</p> <p>LO 4: Determine the limitations of current CMOS structures and alternatives.</p> <p>LO 5: Extend knowledge of dynamic performance to more complex logic structures and systems.</p> <p>LO 6: Demonstrate the fundamental principles of system design.</p> <p><b>Graduate Attributes: levels of attainment</b></p> <p>To act responsibly - Enhanced</p> <p>To think independently - Enhanced</p> <p>To develop continuously - Enhanced</p> <p>To communicate effectively - Enhanced</p> |

<sup>1</sup> [An Introduction to Module Design](#) from AISHE provides a great deal of information on designing and re-designing modules.

<sup>2</sup> [TEP Glossary](#)

**Module Content**

Please provide a brief overview of the module of no more than 350 words written so that someone outside of your discipline will understand it.

- **The MOSFET:** Physical principles of device operation; current voltage relationships, device models; second order effects.
- **Static Circuit Analysis:** MOS inverters; the CMOS inverter transfer characteristic and its switching level; NAND and NOR gates; noise margin; transmission gate.
- **Dynamic Circuit Analysis:** Circuit lay-out, MOS transistor capacitances; inverter step response; gate delays; power dissipation.
- **Technology Scaling, 14 Nanometers and Beyond:** Limitations and emerging technologies. FinFETs.
- **CMOS Logic Functions:** Generalised CMOS combinational logic; XOR and transmission gate logic; sequential logic elements, SRAM, DRAM.
- **CMOS Subsystem Performance:** RC gate delay models.

**Teaching and Learning Methods**

e.g., lectures, seminars, online learning via VLE, field trips, laboratories, practice-based etc...

This module is taught using a combination of lectures, tutorials and two supporting laboratories. During the tutorials, students will develop their problem solving skills by tackling problems based on the lecture material.

**Assessment Details<sup>3</sup>**

Please include the following:

- Assessment Component
- Assessment description
- Learning Outcome(s) addressed
- % of total
- Assessment due date

| Assessment Component | Assessment Description | LO Addressed | % of total | Week due        |
|----------------------|------------------------|--------------|------------|-----------------|
| Written Exam         | Written Exam           |              | 80         | End of Semester |
| Laboratory           | Laboratory             |              | 20         | During Semester |
|                      |                        |              |            |                 |
|                      |                        |              |            |                 |

**Reassessment Requirements**

Supplemental Written Exam

**Contact Hours and Indicative Student Workload<sup>3</sup>**

**Contact hours:**  
36 hours

<sup>3</sup> [TEP Guidelines on Workload and Assessment](#)

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|   | <p><b>Independent Study (preparation for course and review of materials):</b><br/>35</p> <hr/> <p><b>Independent Study (preparation for assessment, incl. completion of assessment):</b><br/>40</p>   |
| <b>Recommended Reading List</b>   | <p>CMOS Digital Integrated Circuits: Analysis and Design, SM Kang and Y Leblebici, McGraw-Hill, 1996.</p> <p>CMOS VLSI Design: a circuits and systems perspective, 4th ed., Neil Weste and David Harris, Pearson Addison Wesley, 2011.</p> <p>Device Electronics for Integrated Circuits, Richard Muller and Theodore Kamins, John Wiley, 2003.</p> |
| <b>Module Pre-requisite</b>   | EEU33C03 or equivalent  |
| <b>Module Co-requisite</b>  |   |
| <b>Module Website</b>   | See Blackboard  |
| <b>Are other Schools/Departments involved in the delivery of this module? If yes, please provide details.</b> | No  |
| <b>Module Approval Date</b>   |   |
| <b>Approved by</b>  |   |
| <b>Academic Start Year</b>  | 2020  |
| <b>Academic Year of Date</b>  | 2019/2020   |