Module Code	EEP55C32
Module Name	VLSI Design
ECTS Weighting[1]	5 ECTS
Semester taught	Semester 2
Module Coordinator/s	Assistant Prof George Floros
Module Learning Outcomes with reference to the Graduate Attributes and how they are developed in discipline	On successful completion of this module, students should be able to: LO1. familiarize themselves with open-source/industrial flows for circuit design, from RTL to GDSII LO2. to use design tools as an experienced user, and to comprehend changes undergone by the circuit while optimized for area, performance or power consumption LO3. gain insight into the design issues of timing, performance, power consumption, verification and test LO4. become knowledgeable enough so as to be able to work as a junior VLSI engineer in an corporate environment using EDA tools **Graduate Attributes: levels of attainment** To act responsibly - Attained To think independently - Attained To develop continuously - Attained To communicate effectively - Enhanced
Module Content	The goals of the course include (1) the presentation and in-depth discussion of design implementation and test methodologies for VLSI systems, (2) getting to grips with the relevant theoretical and practical issues, processes and flow standards, and (3) gaining practical experience actually using ASIC design tools. In the course, design and implementation tools are presented, which begin with the circuit in High Level Description (HDL) format, and produce a complete floorplanning and placement of the circuit in the form needed for delivery at a fab.
Teaching and Learning Methods	

[1] TEP Glossary

Assessment Details[2]
Please include the following:

- **Assessment Component**
- **Assessment description**
- **Learning Outcome(s) addressed**
- **% of total**
- **Assessment due date**

Assessment Component	Assessment Description	LO Addressed	% of total	Week due
Written Exam	2-hr in-person exam	LO1, LO3, LO4	30	Exam Period
Design Exercises	VLSI Design flow (synthesis, placement and route)	LO2, LO3, LO4	70	Announced in the class

Reassessment Requirements

100% based on exam

Contact Hours and Indicative Student Workload[2]

Contact hours: 44 (22 hour lectures, 22 hour labs) with additional hours arranged regularly to support with queries on ongoing assignments
Independent Study (preparation for course and review of materials): 2 hours per week for lecture, total 24 hours
Independent Study (preparation for assessment, incl. completion of assessment): average 4-5 hours per week for the completion of lab exercises, total 44-55 hours

Recommended Reading List

- Jan M. Rabaey, Anantha P. Chandrakasan, and Borivoje Nikolić. Digital integrated circuits: a design perspective. Pearson Education, Incorporated., 2003.
- Kahng, Andrew B., et al. VLSI physical design: from graph partitioning to timing closure. Vol. 312. Netherlands: Springer, 2011.
- Bhatnagar, Himanshu. "Advanced ASIC Chip Synthesis Using Synopsys® Design Compiler™ Physical Compiler™ and PrimeTime®[electronic resource]."

Module Pre-requisite

4C1 Integrated Systems Design or equivalent

Module Co-requisite

Module Website

On Blackboard

[2] TEP Guidelines on Workload and Assessment

Are other Schools/Departments involved in the delivery of this module? If yes, please provide details.	No
Module Approval Date	
Approved by	Prof. Naomi Harte
Academic Start Year	September 2025
Academic Year of Date	2025/26