Urooj Tariq

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Summary

Currently working on the design of energy-efficient models for next-generation communication networks,with a focus on Open RAN (O-RAN) architectures. My research explores power consumption across network components and aims to support more sustainable, scalable systems. I have nearly three years of experience in FPGA-based algorithm development and hardware design for wireless communication systems.This background allows me to approach system-level challenges with both practical insight and academic perspective.I'm interested in contributing to next generation communication systems while continuing to learn and grow in areas like hardware-software integration and energy-efficient design.

Education

CONNECT Center,Trinity college Dublin   *Dublin,Ireland*

PH.D IN ELECTRICAL ENGINEERING   *Cont. Sep. 2022*

- Design and analysis of power consumption models for Open-RAN architectures", Accepted in ICC GreenNet Workshop, 2025.

National University of Science and Technology   *Islamabad, Pakistan*

M.S. IN ELECTRICAL ENGINEERING   *Aug. 2021*

- Master Thesis "Blockchain Mempool memory optimization using Bloom Filter".

Air University   *Islamabad, Pakistan*

B.S. IN ELECTRICAL ENGINEERING   *Aug. 2017*

Presentation

ADVANCE CRT SFI Research Colloquium   *Tralee, Ireland*

POSTER PRESENTATION   *April. 2024*

- Presented my Research work Poster.

CONNECT Plenary   *Clonmel, Ireland*

TALK & POSTER   *May. 2024*

- Delivered a talk and presented a poster about my research work.

IEEE President Series   *Dublin, Ireland*

POSTER PRESENTATION   *Oct. 2024*

- Presented my Research work Poster.

Engineering Research Symposium   *Dublin, Ireland*

TALK & POSTER   *Oct. 2024*

- Presented my Research work Poster.

Work Experience

National Scientific Engineering and Trading Services (NSETS)   *Islamabad, Pakistan*

LEAD DESIGN RESEARCH OFFICER   *Jun. 2021 - Jun. 2022*

- Development of customize FPGA boards for Communication systems.
- Testing and verification of FPGA boards.
- Technical documentation for hardware evaluation and verification.

Air University   *Islamabad, Pakistan*

HARDWARE DESIGN RESEARCH OFFICER   *Jan. 2018 - Jun. 2021*

- Verilog Implementation of system specific communication and transmission related algorithms and standard interfaces, i.e. UDP Gigabit Ethernet Gigabit Ethernet with RTL8211E-VL Phy, ONFI protocol with NAND flash and microcontroller, SPI, I2C for Flash memory and EEPROM, UART RS-232 and RS-422, and 24-bit Sigma DSP audio Codec ADAU 1761.
- Design and implemented a complete system solution in accordance with the user requirement specification
- Data analysis and acquisition for hardware Implementation to update and enhance system performance.
- Trouble shooting and designing a test lab setup of hardware systems in the field.
- Collaboration with other companies for system development and integration.
- Technical documentation for hardware evaluation and verification to ensures intended working of system.