Module Template for New and Revised Modules[1]

Module Code	**EEU44C01**
Module Name	4C1 Integrated Systems Design
ECTS Weighting[2]	5 ECTS
Semester taught	Semester 1
Module Coordinator/s	Shreejith Shanker
Module Learning Outcomes with reference to the Graduate Attributes and how they are developed in discipline	On successful completion of this module, students should be able to: 1. Build a synchronous DSP system in Verilog and verify its performance. 2. Build and test complex FSMs in Verilog. 3. Automate testbenches for automatic pass/fail. 4. Analyse finite precision effects in digital filters. 5. Make design decisions for fixed point implementations given constraints. 6. Analyse memory usage/requirements for FPGA realisations. 7. Target sequential designs to FPGA hardware. **Graduate Attributes: levels of attainment** To act responsibly - Attained To think independently - Attained To develop continuously - Attained To communicate effectively - Enhanced
Module Content	Please provide a brief overview of the module of no more than 350 words written so that someone outside of your discipline will understand it. • Finite state machines with data path. • Verilog HDL language. • Automation of test benches and design of golden vectors. • Code coverage. • Finite precision effects and choice of bit-width in fixed-point applications. • Translating DSP systems designed in MATLAB onto an FPGA. • Memory on FPGAs. • Working with FPGA board peripherals. • Realisation of the above concepts in hardware designs.

[1] An Introduction to Module Design from AISHE provides a great deal of information on designing and re-designing modules.
[2] TEP Glossary

Teaching and Learning Methods	This is a highly practical module. There will be two "classic" style lectures as well as a two-hour practical session each week which will be a lecture/laboratory slot. The FPGA board used to support the practical sessions is the PYNQ-Z2 board. The practical sessions will require the students to complete **3 or 4** assignments outside class hours (average 4 hours extra per week), spreading the load through the year. It is critical that the student keeps up with the practical work during the semester.

Assessment Details[3]
Please include the following:

- **Assessment Component**
- **Assessment description**
- **Learning Outcome(s) addressed**
- **% of total**
- **Assessment due date**

Assessment Component	Assessment Description	LO Addressed	% of total	Week due
Written Exam	End of year exams	2,4,5,6	70	
Lab & Design exercises	FPGA design lab	1,2,7	30	Announced in lab

Reassessment Requirements

100% Based on Exam

Contact Hours and Indicative Student Workload[3]

Contact hours:
44 (22 hour lectures, 22 hour labs)

Independent Study (preparation for course and review of materials):
2 hour / week for lecture review/self study [24]

Independent Study (preparation for assessment, incl. completion of assessment):
2 hours lab prep (formative) [44]

[3] TEP Guidelines on Workload and Assessment

Recommended Reading List	· Verilog HDL, 2nd edition, Palnitkar (reference only). · FPGA Prototyping By Verilog Examples: Xilinx Spartan-3 Version, Pong P Chu, Wiley. · Exploring Zynq MPSoC with PYNQ and Machine Learning Applications, L. Crockett, D. Northcote, C. Ramsay, F. Robinson, B. Stewart, University of Strathclyde.
Module Pre-requisite	EE3C7 or equivalent
Module Co-requisite	
Module Website	On Blackboard
Are other Schools/Departments involved in the delivery of this module? If yes, please provide details.	
Module Approval Date	
Approved by	
Academic Start Year	September 2023
Academic Year of Date	2023/2024