## Module Template for New and Revised Modules

<table>
<thead>
<tr>
<th>Module Code</th>
<th>EEU33C03</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module Name</td>
<td>Analogue Circuits</td>
</tr>
<tr>
<td>ECTS Weighting²</td>
<td>5 ECTS</td>
</tr>
<tr>
<td>Semester taught</td>
<td>Semester 2</td>
</tr>
<tr>
<td>Module Coordinator/s</td>
<td>Prof. Justin King</td>
</tr>
</tbody>
</table>

### Module Learning Outcomes with reference to the Graduate Attributes and how they are developed in discipline

On successful completion of this module, students should be able to:

1. Discuss simplified diode and MOSFET transistor models along with their range of applicability and limitations
2. Discuss the theoretical basis for active filters and be able to choose an appropriate filter type to solve a given problem
3. Identify an appropriate analysis technique and apply it to a given circuit
4. Design diode, transistor and active filter circuits to meet given specifications

**Graduate Attributes: levels of attainment**

To act responsibly - Not embedded
To think independently - Enhanced
To develop continuously - Enhanced
To communicate effectively - Enhanced

### Module Content

This module provides a thorough foundation in the analogue circuits used for processing general signals which are continuous functions of time. The module aims to provide students with knowledge of the operational principles and practical limitations of analogue circuits at device and circuit level, as well as instructing them in the analysis and design of these circuits. All the principles and techniques learned are applicable to the design of analogue systems on a wider scale. During the module, students will develop the analytical and synthesis skills needed to design analogue circuits for electronic equipment intended for any modern application area. Students will, via laboratory sessions, obtain hands-on experience in the design, construction and measurement of practical discrete analogue circuits.

### Teaching and Learning Methods

- Lectures
- Tutorials
- Problem Sets
- Online “Test Your Understanding” formative problems

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1. [An Introduction to Module Design](#) from AISHE provides a great deal of information on designing and re-designing modules.
2. [TEP Glossary](#)
Assessment Details

Please include the following:

- Assessment Component
- Assessment description
- Learning Outcome(s) addressed
- % of total
- Assessment due date

<table>
<thead>
<tr>
<th>Assessment Component</th>
<th>Assessment Description</th>
<th>LO Addressed</th>
<th>% of total</th>
<th>Week due</th>
</tr>
</thead>
<tbody>
<tr>
<td>Written Exam</td>
<td>Written Exam</td>
<td>All</td>
<td>70</td>
<td>End of Semester</td>
</tr>
<tr>
<td>Laboratory</td>
<td>Practical</td>
<td>4</td>
<td>20</td>
<td>9 - 11</td>
</tr>
<tr>
<td>Midterm Exam</td>
<td>MCQ</td>
<td>1, 3</td>
<td>10</td>
<td>6</td>
</tr>
</tbody>
</table>

Reassessment Requirements

Written Exam (100%)

Contact Hours and Indicative Student Workload

- Contact hours: 33
- Independent Study (preparation for course and review of materials): 20
- Independent Study (preparation for assessment, incl. completion of assessment): 55

Recommended Reading List

- Active and Passive Analog Filter Design L. P. Huelsman (McGraw-Hill)

Module Pre-requisite

EEU22E06 or equivalent

Module Co-requisite

Module Website

Blackboard

Are other Schools/Departments involved in the delivery of this module? If yes, please provide details.

No

Module Approval Date

Approved by

Academic Start Year

2022

Academic Year of Date

September 2023

3 TEP Guidelines on Workload and Assessment