The School of Engineering

BAI Electronic Engineering (C Stream)

BAI Computer Engineering (D Stream)

BAI Electronic & Computer Engineering (CD Stream)

Senior Sophister Handbook

2017 – 2018
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Overview

Welcome to the Senior Sophister year of the Integrated BAI/MAI degree programme in the specialisations: Electronic, Electronic & Computer Engineering and Computer Engineering. As you will know by now, these are referred to as the C Stream, CD Stream and D Stream, respectively. The objective of the BAI/MAI degree offered by the Departments of Electronic & Electrical Engineering and Computer Science is to produce well-rounded graduates, having a strong grounding in analytical skills and the flexibility to adapt to the advances in electronic technology, computer systems and communications systems. Having completed one year of specialisation in your chosen discipline you now enter the fourth year of your programme to continue that specialisation towards a Level 8 honours degree. On successful completion of this year with the appropriate grade, you will be eligible to proceed to the 5th Masters year of the programme to compete for the Level 9 MAI degree. Those registered for the MAI degree will not be conferred with their BAI degree until graduating from the MAI year at which point they will receive both the BAI and MAI degrees together. However, students may opt to finish the programme at the Level 8 honours degree and on successful completion of their Senior Sophister year will be awarded the BAI degree. The Senior Sophister year is different from any other year of the programme in that there are several different modes of undertaking the year’s study, depending on the student’s intentions with respect to the MAI degree. The complete details of each mode are outlined below. The information presented in this handbook is as accurate and as complete as possible at the time of going to press but may be subject to some minor changes throughout the course of the academic year. Information not available at the time of going to press will be issued at the appropriate point later in the
year as soon as it becomes available. May we wish you every success in your studies and efforts in your Senior Sophister year.

Contacts:

SS BAI Year Coordinators
Dr M. J. Burke, Dept. of Electronic & Electrical Engineering, mburke@tcd.ie
Dr M. Brady, Dept. of Computer Science, brady@cs.tcd.ie

Academic Registry
Should you need to contact the College Academic Registry please use one of the following means:
- Log an enquiry via ASK AR on the my.tcd.ie portal
- Via email at academic.registry@tcd.ie
- Via phone at (01)8964500 [students] or #4501 [staff]

Programme Structure

BAI Degree Exit
Senior Sophister students who have not opted, or are not eligible, to progress to the MAI programme may complete the SS year to obtain the BAI degree. These students essentially follow the same structure as Mode 1 of the MAI programme. Students take taught modules totalling 45 ECTS and undertake an individual project worth 15 ECTS. Taught modules include 4E1 Management for Engineers in the first semester and 8 other 5 ECTS modules, spread over the two semesters. Modules totalling 30 ECTS are taken in each semester. The individual project dissertation must be submitted towards the end of the second semester.
MAI Degree Modes

Eligible students who have elected to complete the MAI programme follow one of three modes in their Senior Sophister year.

Mode 1

Students completing the year by Mode 1 spend both semesters in Trinity College. Students take taught modules totalling 45 ECTS and undertake an individual project worth 15 ECTS. Taught modules include 4E1 Management for Engineers in the first semester and 8 other 5 ECTS modules, spread over the two semesters. Modules totalling 30 ECTS are taken in each semester. The individual project dissertation must be submitted towards the end of the second semester (date to be confirmed).

Mode 2

Students spend the first semester in Trinity College and take 4E1 Management for Engineers and 5 other 5 ETCS taught modules. In the second semester students complete an industry-based internship, 4E4, worth 30 ECTS. This requires several submissions for assessment including a final dissertation and an oral presentation of the work carried out during or following the internship. Students following Mode 2 will have two internship supervisors: a staff member of the host institution and a member of their parent TCD Department’s academic staff. Students must obtain a II.1 grade or higher in their first attempt at the annual examinations in their Junior Sophister year in order to be eligible to apply for an internship.

Mode 3

Students who obtain a II.1 grade or higher in their first attempt at the annual examinations in their Junior Sophister year may opt to spend their fourth year of study on the Cluster or Unitech programmes in a partner University, or on an Erasmus exchange.
Students who wish to follow Mode 3 must apply through the School of Engineering and obtain approval. It is also essential that the precise programme of study undertaken abroad in Mode 3 is agreed with the students’ parent department(s) to ensure that prerequisites for entry into the MAI year on their return to College are met. More details of study abroad can be found on the School of Engineering website at the following link:

https://www.tcd.ie/Engineering/undergraduate/study-abroad/

The School of Engineering coordinator for the Cluster and Unitech programmes is Prof. B. Broderick, BBRODRCK@tcd.ie. The 5th year MAI coordinator in the Dept. of Electronic & Electrical Engineering is Prof. Anil Kokaram Anil.Kokaram@tcd.ie and in the Dept. of Computer Science is Dr. Mike Brady brady@cs.tcd.ie.

**Academic Year Organization**

The Senior Sophister teaching year is arranged into two 12-week semesters as defined by the College’s academic year outlined in more detail below. The crucial dates are as follows:

**Teaching Weeks:**


**Reading/Study Weeks:**


**Examination Periods:**

Winter examinations for those modules taught wholly in the first semester commence on Tues 2nd January 2018.
Annual examinations commence on Monday 30\textsuperscript{st} April 2018 and finish at the latest on Friday 25\textsuperscript{th} May 2018.

A one-page layout showing the structure of the academic year can be found at the following link:

http://www.tcd.ie/Engineering/undergraduate/pdf/AcademicYearStructure.pdf

**Modules**

Modules are available from both departments involved in teaching the C, CD and D Streams and permitted combinations are detailed below for each stream. Module descriptors which give details of the learning outcomes, syllabi, assignments and assessment methods for each module are no longer included in the handbooks. These are published instead on the School of Engineering website at:

http://www.tcd.ie/Engineering/undergraduate/baiyear4/electroniccomputer/
http://www.tcd.ie/Engineering/undergraduate/baiyear4/computer/

**ECTS**

The European Credit Transfer and Accumulation System (ECTS) is an academic credit system based on the estimated student workload required to achieve the objectives and learning outcomes of a module or programme of study. It is designed to enable academic recognition for periods of study, to facilitate student mobility and credit accumulation and transfer. The ECTS is the recommended credit system for higher education in Ireland and across the European Higher Education Area.
The ECTS weighting for a module is a measure of the student input or workload required for that module, based on factors such as the number of contact hours, the number and length of written or verbally presented assessment exercises, class preparation and private study time, laboratory classes, examinations, clinical attendance, professional training placements, and so on.

For more information and ECTS documentation, see the EU Commission website at:


Modules available to Senior Sophister students, their ECTS credit value and the semesters in which they are taught are as follows:

**School Modules**

<table>
<thead>
<tr>
<th>School</th>
<th>Modules</th>
<th>Semester</th>
<th>ECTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>4E01</td>
<td>Management for Engineers</td>
<td>I</td>
<td>5</td>
</tr>
<tr>
<td>4E02</td>
<td>Individual SS Project</td>
<td>II</td>
<td>15</td>
</tr>
<tr>
<td>4E04</td>
<td>Industrial Internship</td>
<td>II</td>
<td>30</td>
</tr>
</tbody>
</table>

**EEE Modules**

<table>
<thead>
<tr>
<th>EEE</th>
<th>Modules</th>
<th>Semester</th>
<th>ECTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>EE4C04</td>
<td>Next Generation Networks</td>
<td>I</td>
<td>5</td>
</tr>
<tr>
<td>EE4C05</td>
<td>Digital Signal Processing</td>
<td>I</td>
<td>5</td>
</tr>
<tr>
<td>EE4C07</td>
<td>Information and Communication Theory</td>
<td>I</td>
<td>5</td>
</tr>
<tr>
<td>EE4C08</td>
<td>Digital Media Processing</td>
<td>I</td>
<td>5</td>
</tr>
<tr>
<td>EE4C15</td>
<td>Analogue Signal Processing</td>
<td>II</td>
<td>5</td>
</tr>
<tr>
<td>EE4C16</td>
<td>Machine Learning &amp; Media Engineering</td>
<td>I</td>
<td>5</td>
</tr>
<tr>
<td>ME4B09</td>
<td>Control Engineering I</td>
<td>II</td>
<td>5</td>
</tr>
<tr>
<td>ME4B12</td>
<td>Acoustics</td>
<td>II</td>
<td>5</td>
</tr>
<tr>
<td>CS Modules</td>
<td>Semester</td>
<td>ECTS</td>
<td></td>
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<tr>
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<tr>
<td>CS4D2A/CS3041 Information Management II</td>
<td>I</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS3421 Computer Architecture II</td>
<td>I</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS4052 Computer Graphics</td>
<td>I</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS4053 Computer Vision</td>
<td>I</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS4D2B Knowledge Engineering</td>
<td>II</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS7434 Augmented Reality</td>
<td>II</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS4400 Internet Applications</td>
<td>I</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS4404 Machine Learning &amp; Data Analysis</td>
<td>I</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS4405 Optimisation Algorithms for Data Analysis</td>
<td>II</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS4406 Data Visualisation</td>
<td>II</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>CS4407 Security &amp; Privacy</td>
<td>II</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

These modules are summarised in the following table:

<table>
<thead>
<tr>
<th>EEE Modules</th>
<th>CS Modules</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semester 1</td>
<td>Semester 2</td>
</tr>
<tr>
<td>4C4</td>
<td>4C8</td>
</tr>
<tr>
<td>4C5</td>
<td>4C15</td>
</tr>
<tr>
<td>4C7</td>
<td>4B9</td>
</tr>
<tr>
<td>4C16</td>
<td>4B12</td>
</tr>
<tr>
<td>Semester 1</td>
<td>Semester 2</td>
</tr>
<tr>
<td>4D2A/CS3041</td>
<td>CS4D2B</td>
</tr>
<tr>
<td>CS3421</td>
<td>CS7434</td>
</tr>
<tr>
<td>CS4052</td>
<td>CS4405</td>
</tr>
<tr>
<td>CS4053</td>
<td>CS4406</td>
</tr>
<tr>
<td>CS4000</td>
<td>CS4407</td>
</tr>
<tr>
<td>CS4404</td>
<td></td>
</tr>
</tbody>
</table>
Stream Combinations

C Stream
In Semester 1 students following **Mode 1** and **Mode 2** take the following modules 4E1, 4C4, 4C5, 4C7, 4C16 and CS3421.

In Semester 2 students following **Mode 1** take modules 4E2 (project), 4C15 and two 5 ECTS subjects from, 4C8, 4B9, 4B12 and CS4405.

In Semester 2 students following **Mode 2** take the module 4E4 (Industrial Internship)

CD Stream
Students following **Mode 1** take the modules 4E1, 4E2 (Project), 4C4, 4C5 and 6 other 5 ECTS modules over the two semesters with a total of 30 ECTS in each semester. At least 2 modules (a total of 10 ECTS) must be taken from Computer Science.

Students following **Mode 2** take the module 4E1, 4C4, 4C5 and 3 other 5 ECTS modules in Semester 1, including at least 2 modules (a total of 10 ECTS) from Computer Science. The module 4E4 (Industrial Internship) is then taken in Semester 2.

Students following **Mode 1** and **Mode 2** in the CD Stream who intend to proceed to the 5th MAI year must ensure that they choose modules in the SS year that fulfil any prerequisites for the subjects they intend to take in the MAI year. This is the students’ responsibility.
**D Stream**
In Semester 1 students following **Mode 1** and **Mode 2** take the module 4E1, and 5 other CS modules of 5 ECTS each, totalling 25 ECTS credits.

In Semester 2 students following **Mode 1** take the module 4E2 (Project) and three other CS module of 5 ECTS each totalling 15 ECTS credits.

In Semester 2 students following **Mode 2** take the module 4E4 (Industrial Internship).

**Submission Dates**
Subjects such as the Individual Project, 4E02, or the Engineering Project Internship, 4E04, are assessed entirely by continuous assessment. These have a number of elements which must submitted or presented and the associated deadlines in terms of the Semester structure are given below: Please note that some of these dates may change if unforeseen circumstances arise which require it.

**4E02 Individual Project in Dept. of Electronic & Electrical Eng.**
Project Summary: end week 1, Semester 2, Friday 19th January 2018.
Poster File: end week 10, Semester 2, Friday 23rd March 2018.
Presentation Session: during week 11 of Semester 2, date TBC.
Project Report: end of week 12 of Semester 2, Friday 6th April 2018.
**4E02 Individual Project in the School of Computer Science and Statistics**

*Note: these dates are provisional and may be changed:*

Project Demonstration: April 3 – April 6, 2018 (Week 12, Semester 2)

Project Report: Thursday May 3, 2018

Full Details at: [https://www.scss.tcd.ie/StudentProjects/](https://www.scss.tcd.ie/StudentProjects/)

**4E04 Engineering Internship, Dept. Electronic & Electrical Eng**

Takes Place: Monday, 15th January 2018 – Friday, 27th July 2018.


Midway Report: end of week 12, Semester 2, Friday 6th April 2018.


Reflective Diary: Friday 27th July 2018.

Oral Presentation: Friday 31st August 2018, date provisional TBC.

**4E04 Engineering Internship, School of Computer Science and Statistics**

Takes Place: Monday, January 22 2018 - Friday, August 10 2018.


Midpoint submission of Reflective Diary: Friday, April 27, 2018.

Final Report Submission Date: Tuesday, August 7, 2018.

Final Submission of Reflective Diary: Tuesday, August 7, 2018.

Oral Presentation: to be arranged in conjunction with the host – see handbook.

Full details and handbook at: [https://www.scss.tcd.ie/internships/](https://www.scss.tcd.ie/internships/)

**Electronic Engineering Laboratories**

Practical Laboratories will take place in the Department of Electronic & Electrical Engineering, generally on Friday mornings. There will be a varying number of laboratory sessions associated with each module
offered by the EEE department. Some modules may have laboratory sessions built in to their lecture schedule. The timetable for scheduled laboratories is given below. Please note that some laboratories are run by the Dept. of Mechanical Engineering and will therefore take place in the Parsons Building.
# Senior Sophister Dept. EEE Electronics Laboratory Schedule 2017-18

## Semester I Schedule

4C5 Digital Signal Processing, 4C7 Information & Communication Theory, CAD/PC Lab, 2nd Floor, Aras an Phiarsaigh.

<table>
<thead>
<tr>
<th>Friday Mornings</th>
<th>Week 1 29th Sep</th>
<th>Week 2 6th Oct</th>
<th>Week 3 13th Oct</th>
<th>Week 4 20th Oct</th>
<th>Week 5 27th Oct</th>
<th>Week 6 3rd Nov</th>
<th>Week 7 10th Nov</th>
<th>Week 8 17th Nov</th>
<th>Week 9 24th Nov</th>
<th>Week10 1st Dec</th>
<th>Week11 8th Dec</th>
<th>Week12 15th Dec</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.00-11.00</td>
<td>416 C, CD, D, Bio</td>
<td>4C16 C, CD, D, Bio</td>
<td>4C5 C, CD</td>
<td>4C5 C, CD</td>
<td>Reading Week</td>
<td>4C5 C, CD</td>
<td>4C5 C, CD</td>
<td>4C5 C, CD</td>
<td>4C16 C, CD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11.00-13.00</td>
<td>4C16 C, CD, D, Bio</td>
<td>4C16 C, CD, D, Bio</td>
<td>4C5 Bio</td>
<td>4C7 C, CD</td>
<td>4C5 Bio</td>
<td>Reading Week</td>
<td>4C5 Bio</td>
<td>4C5 Bio</td>
<td>4C7 C, CD</td>
<td>4C16 C, CD</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Semester II Schedule

4B9 Control Engineering, Mechanical Engineering Dept., Mechatronics Laboratory, 4th Floor, Parsons Building.
4B12 Acoustics, Mechanical Engineering Dept., Fluids Laboratory, 3 Floor, Parson’s Building.
4C15 Analogue Signal Processing, EEE Dept., Undergraduate Laboratory, 2nd Floor, Aras an Phiarsaigh.

<table>
<thead>
<tr>
<th>Friday Mornings</th>
<th>Week 1 19th Jan</th>
<th>Week 2 25th Jan</th>
<th>Week 3 2nd Feb</th>
<th>Week 4 9th Feb</th>
<th>Week 5 16th Feb</th>
<th>Week 6 23rd Feb</th>
<th>Week 7 2nd Mar</th>
<th>Week 8 9th Mar</th>
<th>Week 9 16th Mar</th>
<th>Week10 23rd Mar</th>
<th>Week11 30th Mar</th>
<th>Week12 6th Apr</th>
</tr>
</thead>
</table>
Attendance
Please note that attendance at lectures, tutorials and laboratory sessions is mandatory as is the submission of all work subject to continuous assessment. Students who prove lacking in any of these elements may be issued with a Non-Satisfactory form and asked for an explanation for their poor attendance or performance. Students who do not provide a satisfactory explanation can be prevented from sitting the annual examinations.

Collaboration and Individual Work
Engineering is about co-operation, but also individual effort. The everyday products of engineering, such as a jet aircraft, a suspension bridge, a DVD player, or a computer have all been designed and built by teams of dozens, hundreds and even thousands, of engineers working together. These engineers exchange ideas and ultimately co-ordinate their efforts to achieve the overall project goal. However, each component of even the largest project is the result of one individual’s engineering skill and imagination.

If you want to become a successful engineer, you must develop your own ability to analyse problems. This means that, while it is useful to work as a team initially, you must ultimately produce your own work. For example, in the case of a computing exercise, discuss the task with your classmates, swap ideas on how to solve the problem, but at the end of the day, you must be able to implement your own solution. The examinations will test your ability to apply your skills rather than just acquired knowledge and the only way to develop your ability for engineering analysis is to complete the laboratory experiments, tutorial exercises and design or analysis assignments yourself.
**Plagiarism**

In the academic world, the principal currency is *ideas*. As a consequence, you can see that plagiarism – i.e. passing off other people’s ideas as your own – *is tantamount to theft*. It is important to be aware that plagiarism can occur knowingly or unknowingly, and the offence is in the action not the intent.

Plagiarism is a serious offence within College and the College’s policy on plagiarism is set out in a central online repository hosted by the Library which is located at [http://tcd-ie.libguides.com/plagiarism](http://tcd-ie.libguides.com/plagiarism). This repository contains information on what plagiarism is and how to avoid it, the College Calendar entry on plagiarism and a matrix explaining the different levels of plagiarism outlined in the Calendar entry and the sanctions applied.

Undergraduate and postgraduate new entrants and existing students, are required to complete the online tutorial *'Ready, Steady, Write'*. Linked to this requirement, all cover sheets which students must complete when submitting assessed work, must contain the following declaration:

**I have read and I understand the plagiarism provisions in the General Regulations of the University Calendar for the current year, found at:** [http://www.tcd.ie/calendar](http://www.tcd.ie/calendar).

**I have also completed the Online Tutorial on avoiding plagiarism ‘Ready, Steady, Write’, located at:**


Plagiarism detection software such as “Turnitin” and Blackboard’s “SafeAssign” may be used to assist in automatic plagiarism detection. Students are encouraged to examine their own work for plagiarism prior to submission using this or other software.
BAI/MAI Examination Rules

The Examination Regulations in the School of Engineering comply with the College Council approved Harmonisation Regulations and can be found for the Senior Sophister year on the School website at: https://www.tcd.ie/Engineering/undergraduate/pdf/ExaminationRules_15_16.pdf.

Trinity Education Project

The Trinity Education Project is a university wide initiative to ‘rearticulate what a Trinity Education should be in the 21st century and to reemphasise our role as a leader in education’. This will enhance the experience of all Trinity students, including those in the school of engineering. The ‘high level’ graduate attributes span 4 dimensions – academic excellence, critical thinking and effective communication, life-long learning, and global citizenship. The academic and administrative structures will be enhanced to provide student learning-centred assessment, learning spaces, curriculum principles and architecture, internships and study abroad options and technology enhanced learning where appropriate.

While many details in this project have still to be determined, the currently proposed architecture for professional degrees (including engineering) would see 10 ECTS of ‘free electives’ (modules available to all students in the university, and chosen by the students) made available within the first 4 years of the programme, and 20 ECTS of ‘approved modules’ (modules from a prescribed menu outside of the students core requirements, but which are recognized as cognate and coherent). The school of engineering is excited by the opportunities to use this new project to provide flexible and agile responses to the needs of our graduates.

For more detail see https://www.tcd.ie/academic-services/tep/