Module Title: 4C2 Microelectronic Circuits

Code: EEU44C02

Level: Senior Sophister (Mandatory module)

Credits: 5

Lecturer(s): TBD

Module Organisation

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<tr>
<th>Semester</th>
<th>Start Week</th>
<th>End Week</th>
<th>Associated Practical Hours</th>
<th>Lectures</th>
<th>Tutorials</th>
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Total Contact Hours: 48

Module Description
CMOS is the technology driving the semiconductor industry and the digital revolution. It is the technology inside ICs (Integrated Circuits) allowing digital media such as the iPad and mobile phones become sufficiently low-cost, small, and low-power to meet the demands of today's consumers. This module will allow the student to develop a strong understanding of the fundamentals of CMOS, how logic structures are built with CMOS and the challenges involved in the constant scaling to smaller technologies.

Learning Outcomes
On completion of this module, the student will be able to:

1. Explain the electrical operation of the metal-oxide-semiconductor (MOS) field effect transistor;
2. Analyse the fundamental static and dynamic performance of simple CMOS circuits noting design trade-offs;
3. Implement various CMOS logic structures;
4. Determine the limitations of current CMOS structures and alternatives;
5. Extend knowledge of dynamic performance to more complex logic structures and systems;
6. Demonstrate the fundamental principles of system design.
Module Syllabus

- **The MOSFET**: Physical principles of device operation; current voltage relationships, device models; second order effects.
- **Static Circuit Analysis**: MOS inverters; the CMOS inverter transfer characteristic and its switching level; NAND and NOR gates; noise margin; transmission gate.
- **Dynamic Circuit Analysis**: Circuit lay-out, MOS transistor capacitances; inverter step response; gate delays; power dissipation.
- **Technology Scaling, 45 Nanometers and Beyond**: Limitations and emerging technologies.
- **CMOS Logic Functions**: Generalised CMOS combinational logic; XOR and transmission gate logic; sequential logic elements, SRAM, DRAM.
- **CMOS Subsystem Performance**: RC gate delay models.

Associated Laboratory/Project Programme
There will be three associated laboratories which will be used to demonstrate the operation of some of the CMOS circuits studied in the lectures.

Recommended Text(s)


Teaching Strategies
This module is taught using a combination of lectures, tutorials and two supporting laboratories. During the tutorials, students will develop their problem solving skills by tackling problems based on the lecture material.

Assessment
The formal written end-of-year two hour examination will contribute 80% towards overall grade and laboratory reports will contribute the remaining 20%.