<table>
<thead>
<tr>
<th><strong>Module Code</strong></th>
<th>EE5M02</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Module Name</strong></td>
<td>Microelectronic Circuits</td>
</tr>
<tr>
<td><strong>ECTS Weighting</strong></td>
<td>5 ECTS</td>
</tr>
<tr>
<td><strong>Semester taught</strong></td>
<td>Semester 2</td>
</tr>
<tr>
<td><strong>Module Coordinator/s</strong></td>
<td>Dr Justin King</td>
</tr>
</tbody>
</table>

**Module Learning Outcomes with reference to the Graduate Attributes and how they are developed in discipline**

On successful completion of this module, students should be able to:

- **LO 1:** Explain the electrical operation of the metal-oxide-semiconductor (MOS) field effect transistor.
- **LO 2:** Analyse the fundamental static and dynamic performance of simple CMOS circuits noting design trade-offs.
- **LO 3:** Implement various CMOS logic structures.
- **LO 4:** Determine the limitations of current CMOS structures and alternatives.
- **LO 5:** Extend knowledge of dynamic performance to more complex logic structures and systems.
- **LO 6:** Demonstrate the fundamental principles of system design.

**Graduate Attributes: levels of attainment**

- To act responsibly - Enhanced
- To think independently - Enhanced
- To develop continuously - Enhanced
- To communicate effectively - Enhanced

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1. [An Introduction to Module Design](#) from AISHE provides a great deal of information on designing and re-designing modules.
2. [TEP Glossary](#)
Module Content

Please provide a brief overview of the module of no more than 350 words written so that someone outside of your discipline will understand it.

- **The MOSFET**: Physical principles of device operation; current voltage relationships, device models; second order effects.
- **Static Circuit Analysis**: MOS inverters; the CMOS inverter transfer characteristic and its switching level; NAND and NOR gates; noise margin; transmission gate.
- **Dynamic Circuit Analysis**: Circuit lay-out, MOS transistor capacitances; inverter step response; gate delays; power dissipation.
- **Technology Scaling, 14 Nanometers and Beyond**: Limitations and emerging technologies. FinFETs.
- **CMOS Logic Functions**: Generalised CMOS combinational logic; XOR and transmission gate logic; sequential logic elements, SRAM, DRAM.
- **CMOS Subsystem Performance**: RC gate delay models.

Teaching and Learning Methods

e.g., lectures, seminars, online learning via VLE, field trips, laboratories, practice-based etc...

This module is taught using a combination of lectures, tutorials and two supporting laboratories. During the tutorials, students will develop their problem solving skills by tackling problems based on the lecture material.

Assessment Details

<table>
<thead>
<tr>
<th>Assessment Component</th>
<th>Assessment Description</th>
<th>LO Addressed</th>
<th>% of total</th>
<th>Week due</th>
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<tbody>
<tr>
<td>Written Exam</td>
<td>Written Exam</td>
<td></td>
<td>80</td>
<td>End of Semester</td>
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<tr>
<td>Laboratory</td>
<td>Laboratory</td>
<td></td>
<td>20</td>
<td>During Semester</td>
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</table>

Reassessment Requirements

Supplemental Written Exam

Contact Hours and Indicative Student Workload

<table>
<thead>
<tr>
<th>Contact hours:</th>
</tr>
</thead>
<tbody>
<tr>
<td>36 hours</td>
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1 [TEP Guidelines on Workload and Assessment](#)
<table>
<thead>
<tr>
<th>Task</th>
<th>Hours</th>
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</thead>
<tbody>
<tr>
<td>Independent Study (preparation for course and review of materials)</td>
<td>35</td>
</tr>
<tr>
<td>Independent Study (preparation for assessment, incl. completion of assessment)</td>
<td>40</td>
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</table>

**Recommended Reading List**


**Module Pre-requisite**

- EEU33C03 or equivalent

**Module Co-requisite**

- None

**Module Website**

- See Blackboard

**Are other Schools/Departments involved in the delivery of this module?**

- No

**Module Approval Date**

- Approved by

**Academic Start Year**

- 2020

**Academic Year of Date**

- 2019/2020