Module Template for New and Revised Modules[1]

Module Code	**EE5M02**
Module Name	Microelectronic Circuits
ECTS Weighting[2]	5 ECTS
Semester taught	Semester 2
Module Coordinator/s	Prof Phillip Christie
Module Learning Outcomes with reference to the Graduate Attributes and how they are developed in discipline	On successful completion of this module, students should be able to: LO 1: Explain the electrical operation of the metal-oxide-semiconductor (MOS) field effect transistor. LO 2: Analyse the fundamental static and dynamic performance of simple CMOS circuits noting design trade-offs. LO 3: Implement various CMOS logic structures. LO 4: Determine the limitations of current CMOS structures and alternatives. LO 5: Extend knowledge of dynamic performance to more complex logic structures and systems. LO 6: Demonstrate the fundamental principles of system design. **Graduate Attributes: levels of attainment** To act responsibly - Enhanced To think independently - Enhanced To develop continuously - Enhanced To communicate effectively - Enhanced

[1] An Introduction to Module Design from AISHE provides a great deal of information on designing and re-designing modules.
[2] TEP Glossary

Module Content

Please provide a brief overview of the module of no more than 350 words written so that someone outside of your discipline will understand it.

- ***The MOSFET:*** Physical principles of device operation; current voltage relationships, device models; second order effects.
- ***Static Circuit Analysis:*** MOS inverters; the CMOS inverter transfer characteristic and its switching level; NAND and NOR gates; noise margin; transmission gate.
- ***Dynamic Circuit Analysis:*** Circuit lay-out, MOS transistor capacitances; inverter step response; gate delays; power dissipation.
- ***Technology Scaling, 14 Nanometers and Beyond:*** Limitations and emerging technologies. FinFETs.
- ***CMOS Logic Functions:*** Generalised CMOS combinational logic; XOR and transmission gate logic; sequential logic elements, SRAM, DRAM.
- ***CMOS Subsystem Performance:*** RC gate delay models.

Teaching and Learning Methods

e.g., lectures, seminars, online learning via VLE, field trips, laboratories, practice-based etc…

This module is taught using a combination of lectures, tutorials and two supporting laboratories. During the tutorials, students will develop their problem solving skills by tackling problems based on the lecture material.

Assessment Details[3]
Please include the following:

- **Assessment Component**
- **Assessment description**
- **Learning Outcome(s) addressed**
- **% of total**
- **Assessment due date**

Assessment Component	Assessment Description	LO Addressed	% of total	Week due
Written Exam	Written Exam		80	End of Semester
Laboratory	Laboratory		20	During Semester

Reassessment Requirements

Supplemental Written Exam

Contact Hours and Indicative Student Workload[3]

Contact hours:
36 hours

[3] TEP Guidelines on Workload and Assessment

	Independent Study (preparation for course and review of materials): 35
	Independent Study (preparation for assessment, incl. completion of assessment): 40
Recommended Reading List	CMOS Digital Integrated Circuits: Analysis and Design, SM Kang and Y Leblebici, McGraw-Hill, 1996. CMOS VLSI Design: a circuits and systems perspective, 4th ed., Neil Weste and David Harris, Pearson Addison Wesley, 2011. Device Electronics for Integrated Circuits, Richard Muller and Theodore Kamins, John Wiley, 2003.
Module Pre-requisite	EEU33C03 or equivalent
Module Co-requisite	
Module Website	See Blackboard
Are other Schools/Departments involved in the delivery of this module? If yes, please provide details.	No
Module Approval Date	
Approved by	
Academic Start Year	2020
Academic Year of Date	2019/2020