**Module Title:** 4C1 Integrated Systems Design

**Code:** EE4C01

**Level:** Senior Sophister (Mandatory module)

**Credits:** 5

**Lecturer(s):** Assist. Professor Naomi Harte

### Module Organisation

<table>
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<tr>
<th>Semester</th>
<th>Start Week</th>
<th>End Week</th>
<th>Associated Laboratory Hours</th>
<th>Lectures Per week</th>
<th>Total</th>
<th>Practicals Per week</th>
<th>Total</th>
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<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>12</td>
<td>8</td>
<td>2</td>
<td>22</td>
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<td>22</td>
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**Total Contact Hours: 52**

### Module Description

This module builds directly on the 3C7 Digital Systems Design module from the Junior Sophister year. It will introduce more advanced topics in Verilog-based FPGA design. The approach will be from a systems perspective, looking at the implication of design trade-offs for integrated digital systems typical in DSP and consumer applications.

### Learning Outcomes

On completion of this module, the student will be able to:

1. Build a synchronous DSP system in verilog and verify its performance;
2. Build and test complex FSMs in Verilog;
3. Automate testbenches for automatic pass/fail;
4. Analyse finite precision effects in filters;
5. Make design decisions for fixed point implementations given constraints;
6. Analyse memory usage/requirements for FPGA;
7. Target sequential designs to FPGA.

### Module Syllabus

- Finite state machines with datapath;
- Verilog HDL language;
- Automation of testbenches and design of golden vectors;
- Code coverage;
- Finite precision effects and choice of bit-width in fixed-point applications;
- Translating DSP system designed in Matlab onto an FPGA;
- Memory on FPGAs;
- Working with FPGA board peripherals;
- Realisation of all above concepts in hardware designs.
**Associated Laboratory/Project Programme**
Four 2 hour laboratories will be used to support the existing practical element of the module. There will be no extra assignments from these sessions.

**Recommended Text(s)**
- *Digital Design*, 4th edition, MM Mano and MD Ciletti, Digital Design, (Pearson) Prentice Hall, 2007, can be used if it was purchased in second year but be aware that the examples are in VHDL, not in Verilog.

Supplementary reading material may be provided during the module.

**Teaching Strategies**
This is a highly practical module. There will be two “classic” style lectures as well as a two-hour practical session each week which will be a lecture/laboratory slot. The FPGA board used to support the practical sessions is the Spartan-3 starter board. The practical sessions will require the students to complete weekly assignments outside class hours (average 4 hours extra per week), spreading the load through the year. It is critical that the student keeps up with the practical work during the semester.

**Assessment**
The formal written two hour end-of-year examination will contribute 50% of the overall subject mark at the annual and supplemental examination sessions. Practical work from the module will also contribute 50% towards the overall grade. Attendance at weekly practical sessions is compulsory. No marks will be given for the corresponding assignment for unattended practical sessions.

Submission dates will be given for each related assignment.

**Late assignments policy:**
- Lose half of marks if up to 1 week late.
- No marks if over 1 week late.